Amendments to the Claims:

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1. (Currently Amended) A system comprising:

N different memories wherein N> 1;

M different busses with each one of the M different busses having a bandwidth to transport data at a predetermined rate, operatively coupled to each one of the N memories wherein M is greater than 1;

a plurality of different memory controllers with each one of the plurality of different memory controllers operatively coupled to one of the N memories, wherein said each one of the plurality of memory controllers setting an associated different memory in at least a first mode ~~or a second mode~~; and

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[[an]] a single arbiter responsive to at least one ~~memory request~~ signal requesting access to the N different memories wherein said single arbiter [[to]] generates an Access vector that causes information to be read simultaneously from multiple ones of the N different memories ~~memory~~ set in the at least a first mode wherein total bandwidth on selected ones of the M different busses ~~of the multiple ones~~ of the N different memories is greater than the bandwidth on a single bus of the M different busses ~~of one~~ of the N different memories.

2. (Currently Amended) The system of Claim 1 wherein the at least first mode includes a Read mode.

3. (Currently Amended) The system of claims 1 or 2 wherein each of the N different memories includes DDR DRAM.

4. (Currently Amended) The system of claim 3 wherein each of the DDR DRAM ~~are~~ is partitioned into at least four banks and at least one buffer is spread across the at least four banks.

5. (Currently Amended) The system of claim 4 wherein ~~each~~ the at least one buffer is partitioned into multiple maskable units.

6. (Currently Amended) The system of claim 4 wherein ~~each~~ the at least one buffer is partitioned into four units.

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7. (Currently Amended) The system of claim 6 wherein each unit is equivalent to 1/4 the size of the at least one buffer.

8. (Original) The system of claim 6 wherein each unit is maskable.

9. (Currently Amended) The system of claim 1 further including ~~wherein the arbiter includes~~ a controller operatively coupled to said arbiter, said controller executing a ~~slice~~ selection algorithm to select one of the N different memories in which data is to be written said selection algorithm comprising ~~the steps of~~:
   - Exclude slices scheduled for re-fresh cycle (indicated by each DRAM controller)
   - Assign slices for all R requests of Transmitter controller
   - Complement R-accesses from corresponding EPC queue [Slice; QW]
   - Assign slice to EPC for globally W excluded slices (e.g. slice is excluded by all slice exclusion rules from Receiver)

- Assign slices to W requests in RR (Round Robin) fashion between non-excluded slices staring from last assigned slice (slice assigned to Receiver Controller in previous window)
- Complement W-accesses by EPC accesses from corresponding EPC queue [Slice; QW] and
- Assign slice to EPC requests according to priority expressed by Weight.

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24. (Currently Amended) ~~The method of claim 23 further including the acts of an~~ A method comprising:

providing a plurality of separate memory elements in which frames from communication device are to be stored or retrieved;

partitioning at least one of the frames with a controller into at least two parts;

storing each one of the at least two parts into different ones of the plurality of separate memory elements; and

providing a single arbiter [[in]] responsive to a request signal to cause ~~causing~~ the different ones of the ~~memories~~ plurality of separate memory elements to be read simultaneously wherein each one of the ~~two~~ adjoining parts is available simultaneously on respective busses associated with each ~~one~~ of said ones of the plurality of separate memory elements.

25. (Currently Amended) A method including ~~the acts of~~:

providing a plurality of separate memories in which data is stored;

providing a single arbiter to grant access to the plurality of separate memories;

receiving in [[an]] the single arbiter a request to read data from selected ones of said plurality of separate memories; and

simultaneously reading said selected ones of said plurality of separate memories to provide data simultaneously on individual busses coupled to the selected ones of said plurality of separate memories.

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26. (Currently Amended) The method of claim 25 wherein the bandwidth of data on each one of the individual busses is less than the total bandwidth on all activated busses.

27. (Currently Amended) A method comprising ~~the acts of~~:

providing a plurality of separate memory modules in which frames ~~from communication devices can be~~ are being stored;

partitioning a frame into multiple parts;

writing adjacent parts of the frame so partitioned in different ones of the plurality of separate memory modules; and

simultaneously accessing, with a single arbiter, multiple ones of the plurality of separate memory modules in a single memory access window to read data therefrom wherein the total bandwidth of data output from the multiple memory modules matches the bandwidth of a FAT pipe port ~~on~~ associated with a communication device.

28. (Original) The system of claim 9 wherein the controller includes a state machine or other hardware circuits.

29. (New) A system providing data comprising:

a FAT pipe port;

a FIFO buffer for providing data to said FAT pipe port;

a transmit controller;

a single memory arbiter operably coupled to the transmit controller; and

N different memory elements, each one coupled through a separate bus to said single memory arbiter wherein said transmit controller monitors current filling level of data in said FIFO buffer and periodically issuing request signals for data to said single memory arbiter which causes data to be transferred from selected ones of the N different memory elements into the FIFO buffer to ensure data level in said FIFO buffer is being maintained at a level to prevent data underrun at said FAT pipe port.

30. (New) The system of claim 29 wherein at least one of the N different memory elements is partitioned into M sectors, M > 1, and at least one buffer spread across the M sectors.

31. (New) The system of claim 30 wherein the data being transferred into said FIFO buffer is in a buffer size chunk.

32. (New) The system of claim 31 wherein the buffer size chunk is approximately 64 bytes.

33. (New) A system comprising:

N different memory elements, N > 1, wherein at least two of said N different memory elements are each partitioned into multiple sectors and each of the at least two of said N different memory elements so partitioned is partitioned into at least one buffer spread across said multiple sectors;

a plurality of memory controllers with each one of said plurality of memory controllers operatively coupled to each one of the N different memory elements; and

a single arbiter operatively coupled to the plurality of memory controllers, said single arbiter being response to a write request signal to generate a write control signal that causes data to be written in one of the at least one buffer associated with one of the at least two of said N different memory elements.

34. (New) The system of claim 33 further including said single arbiter being responsive to a read request signal to generate a read control signal that causes data to be read from another of the at least one buffer associated with another of the at least two of said N different memory elements.